IN THE SPECIFICATION:

Please amend paragraph number **[0007]** as follows:

[0007] Integrated circuit devices are constructed by ~~making~~ making, e.g., a (silicon or germanium) semiconductor die with internal and surface circuits including transistors, resistors, capacitors, etc. A single semiconductor die may contain thousands of such components and generate considerable heat. Electrical connection pads on an "active" surface of the semiconductor die are connected to the various die circuits. The integrated circuit device also includes electrical leads enabling the electrical connection pads of the semiconductor die to be connected to circuits on a PCB (or other substrate) of an appliance.

Please amend paragraph number **[0013]** as follows:

[0013] In one aspect of the invention, an elastomer is used to cover a portion of a semiconductor die prior to glob top application of the die to the circuit board. The elastomer is removed, e.g., by peeling, from the die surface and includes any glob top material which has inadvertently been applied to the elastomer. Thus, the portion of the semiconductor die remains free of contaminants. If desired, since a portion of the semiconductor die is free of contaminants, providing a good adhesion surface, a heat sink may be attached to such portion of the semiconductor die. The method is applicable to both wire-bonded dice and flip-chip die bonding to circuit boards. ~~Alternately,~~ Alternatively, the elastomer may be retained on a portion of the semiconductor die after the molding or glob-topping of the die for the attachment of a heat sink thereto, if desired. The elastomer may be a highly thermally conductive elastomer to enhance the heat transfer from the semiconductor die to the surrounding environment. An example of a highly thermally conductive elastomer is a metal-filled elastomer or an elastomer filled with a highly thermally conductive material like metal.

Please amend paragraph number **[0029]** as follows:

[0029] In an alternative arrangement, the glob top material 38 may be applied to cover a major portion or all of the heat sink 30. This results in decreased heat dissipation capability, however, but may be used where the thermal output of the semiconductor device permits.

Please amend paragraph number **[0033]** as follows:

[0033] In drawing FIG. 3A, a semiconductor die 12 has an active surface 14 with bond pads 16 near opposing sides of the semiconductor die 12. The back side 18 of the semiconductor die 12 is first bonded to the upper surface 26 of the substrate 20 by a layer of adhesive 40. The substrate 20 may be a printed circuit board (PCB) or other materials such as a flex circuit or ceramic. A layer of a thermally conductive-filled gel elastomer 50 may be either applied to the semiconductor die while in wafer form or subsequently applied to active surface 14 between the arrays of bond pads 16 of the semiconductor die 12 after singulation of the semiconductor die 12 from the wafer. The purpose of the gel elastomer 50 is to provide a protective mask over an area of the semiconductor die 12 to which the heat sink 30 (FIG. 3E) is to be bonded. Alternatively, when a second layer is used as a mask, the first layer may be retained on a portion of the semiconductor die 12 after the molding or glob-topping of the semiconductor die 12 for the attachment of a heat sink thereto, if desired (to be described in FIG. 3C). The gel elastomer 50 is applied as a gel or as a semi-solid or solid coupon. The gel elastomer 50, or a suitable silicon elastomeric material, ~~etc.~~ etc., if the gel elastomer 50 is to be disposed after removal from the semiconductor die 12, or the use of a metal-filled gel elastomer 50, if such is to remain on the semiconductor die 12, may include one or more dams 52 to help prevent the flow of any subsequently applied material from covering the surface of the gel elastomer 50. The dams 52 may extend along one or more sides of the semiconductor die 12, as desired, and may be of any suitable height. The dams 52 may be of any suitable material. Alternatively, the dams 52 may comprise a second layer of gel elastomer 50 having a size smaller than that of the gel elastomer 50. Subsequent glob top application is difficult to precisely control, and any glob top material 38 which lands on the gel elastomer 50 will be later removed by removal of the gel

elastomer from the active surface 14 of the semiconductor die 12. Typically, the gel elastomer 50 may be removed simply by peeling it from the active surface 14 of the semiconductor die 12. Typically, if the gel elastomer 50 is to be removed from the semiconductor die 12 after the glob top material application, a silicon type elastomer may be used on the semiconductor die 12 and removed therefrom for the application of a heat sink to the semiconductor die 12.

Please amend paragraph number **[0035]** as follows:

[0035] In the next step, shown in drawing FIG. 3B, the bond pads 16 are wire bonded to electrical connection pads 24 on the substrate 20 ~~by e.g.,~~ by, e.g., thermosonic, thermocompression or ultrasonic methods, as known in the art.

Please amend paragraph number **[0040]** as follows:

[0040] The particular materials which may be used as die-to-substrate adhesives 40 include those commonly known and/or used in the art. Examples of such are polyimides, a 75% silver-filled cyanate ester paste, an 80% silver-filled cyanate ester paste, and a silver-filled lead glass paste, etc.

Please amend paragraph number **[0042]** as follows:

[0042] As illustrated in drawing FIG. 3F, further glob top material 48 may be applied to the semiconductor device 10, particularly between the existing glob top material 38 and the heat sink 30, for improved sealing. In this figure, the glob top materials 38 and 48 are shown overcovering the substrate 20 between semiconductor device 10 and an adjacent semiconductor device, of which only a connection pad 24A and a bond wire 22A are visible. The semiconductor device 10 is effectively sealed to the substrate 20 to prevent electrical short-circuiting, wire breakage and debonding, and moisture penetration.

Please amend paragraph number **[0045]** as follows:

[0045] The glob top materials 38 and 48 may be the same or different materials. Glob top materials useful for this application include HYSOL™ FP4451 material or HYSOL™ FP4450 ~~high purity, low stress~~ high-purity, low-stress liquid encapsulant material, available from the DEXTER ELECTRONIC MATERIALS DIVISION OF DEXTER CORPORATION, etc.

Please amend paragraph number **[0048]** as follows:

[0048] As depicted in drawing FIG. 4A, a ~~flip chip~~ flip-chip or semiconductor die 12 having an active surface 14 with a grid of electrical connections 56, shown as solder balls, is down bonded to electrical circuit traces 54 (not shown) on an upper surface 26 of a substrate 20. The semiconductor die 12 has an opposing back side 18 and edges 32. The substrate 20 may be a printed circuit board (PCB) or other material such as a flex circuit or ceramic. A layer or coupon of thermally conductive-filled gel elastomer 50, alternatively, a suitable elastomer, silicon elastomeric material, ~~etc.~~ etc., if the gel elastomer 50 is to be discarded, is applied as a solid or semisolid to the back side 18 of the semiconductor die 12, either before or (preferably) after the semiconductor die 12 is electrically down bonded to the substrate 20. The gel elastomer 50 masks the back side 18 from glob top material 38 which may be inadvertently misapplied to the back side 18, requiring removal by erosive blasting or other methods. The use of the gel elastomer 50 obviates such glob top removal methods.

Please amend paragraph number **[0051]** as follows:

[0051] As shown in drawing FIG. 4C, the gel elastomer 50 is then ~~removed~~ removed, e.g., by peeling it from the back side 18 of the semiconductor die 12. The back side 18 of semiconductor die 12 in drawing FIG. 4D is then bare and clean for enhanced attachment of a heat sink 30 thereto.

Please amend paragraph number **[0054]** as follows:

[0054] Alternatively, a room temperature vulcanizing rubber (RTV), which may vary in the degree of thermal conductivity thereof, may be used to completely cover and seal the semiconductor device to the substrate 20, including the glob top material 38.